In the Claims:

1. (Previously presented) An apparatus for predicting a conditional branch outcome within a computer system, the apparatus comprising an activity monitor, responsive to identifying an occurrence of a conditional branch, the activity monitor providing a measure of system activity, indicative of a level of logic state changes, since a previous branch for comparison with data relating to previous system activity, the conditional branch outcome being predicted based on such comparison.

2. (Previously presented) An apparatus according to claim 1, wherein the data relating to system activity comprises average system activity.

3. (Previously presented) An apparatus according to claim 1, wherein an activity history table is provided that stores and associates previous system activity with corresponding outcomes of previous branches.

4. (Previously presented) An apparatus according to claim 3, wherein data relating the system activity between the conditional branch and the previous branches is retrieved for comparison with the data contained in the activity history table, the conditional branch outcome being predicted based on selecting the previous branch outcome associated with activity history data which most closely resembles the retrieved system activity data.

5. (Previously presented) An apparatus according to claim 4, wherein the activity history table is updated based on activity data associated with the conditional branch outcome.

6. (Previously presented) An apparatus according to claim 1, wherein the conditional branch outcome is predicted using outcome history of the conditional branch.

7. (Previously presented) An apparatus according to claim 6, wherein data relating to the activity of the system is only used for branch outcome prediction if confidence of accuracy of branch outcome prediction using branch history is relatively low.

8. (Previously presented) A method for predicting conditional branch outcome within a computer system, the method comprising the steps of identifying an occurrence of a conditional branch, obtaining data providing a measure of system activity, indicative of a level of logic state changes, since a previous branch, comparing said data with data relating to previous system activity, and predicting the conditional branch outcome based on such comparison.

9. (Previously presented) A method according to claim 8, wherein the system activity data is a measure of average system activity.

10. (Previously presented) A method according to claim 9, wherein the average system activity is determined by monitoring a system supply current.

11. (Previously presented) A method according to claim 8, further comprising associating data relating to previous system activity with corresponding outcomes of previous branches, and storing the previous system activity and associated previous branch outcomes in an activity history table.

12. (Previously presented) A method according to claim 11, further comprising retrieving data relating the system activity between the conditional branch and the previous branches, comparing the retrieved data with the data stored in the activity history table, and predicting the conditional branch outcome based on selecting the previous branch outcome associated with activity history data most closely resembling the retrieved system activity data.

13. (Previously presented) A method according to claim 12, further comprising updating the activity history table based on activity data associated with the conditional branch outcome.

14. (Previously presented) A method according to claim 8, further comprising predicting the conditional branch outcome based on outcome history of the conditional branch.

15. (Previously presented) A method according to claim 14, further comprising determining whether to use data relating to the activity of the system for predicting branch outcome based on confidence of accuracy of conditional branch outcome prediction using branch history.

16. (Previously presented) An apparatus according to claim 1, wherein the activity monitor monitors supply current.

17. (Previously presented) An apparatus according to claim 1, wherein the activity monitor includes a series of logic elements including a plurality of sequential logic elements clocked by a clock signal and plurality of combinatorial logic elements connecting the sequential logic elements such that, for a given clock signal cycle, counting state changes within the logic elements provides the measure of system activity.

18. (Previously presented) An apparatus according to claim 17, wherein the sequential logic elements include flip-flops.

19. (Previously presented) An apparatus according to claim 17, wherein the sequential logic elements include D-type latches.

20. (Previously presented) An apparatus according to claim 17, wherein the combinatorial logic elements include processing logic blocks and data path logic blocks.